WHAT IS CLAIMED IS:

1. A matrix calculator for performing multiplication on a first matrix and a second matrix, comprising:

an element selecting portion being input with elements of the first matrix and the second matrix, the element selecting portion for sequentially selecting each of the input elements that will constitute a multiplicand of each sub-element of each element of a multiplication result matrix, and for sequentially outputting the selected said each of the input elements;

a calculating portion for sequentially calculating said each element of the multiplication result matrix by sequentially adding multiplied values of outputs from the element selecting portion;

a storing portion for storing output from the calculating portion; and

a control signal generating portion for generating a control signal that controls a timing of operation of the calculating portion and the storing portion.

2. The matrix calculator of claim 1, wherein the element selecting portion comprises:

a multiplexer being input with the respective elements of the first matrix and the second matrix in parallel; and

a control block for generating a selection signal that selects an output from the multiplexer.

3. The matrix calculator of claim 2, wherein the calculating portion comprises:

a multiplier for multiplying the output from the multiplexer;

a first memory for temporarily storing output from the multiplier;

a second memory; and

an adder for adding a first value stored in the first memory with a second value stored in the second memory, and inputting a resultant value of the adding operation into the second memory.

4. The matrix calculator of claim 3, wherein the control signal generating portion comprises a plurality of flip-flops for generating signals that delay said selection signal output from the control block by a predetermined number of clock pulses, and then inputting the generated signals into the calculating portion and the storing portion.

5. The matrix calculator of claim 4, wherein the storing portion comprises a plurality of registers for sequentially storing the output from the calculating portion.